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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

PHAM, LONG

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Election/Restrictions

Claims 1-18 are pending. Claims 19-20 have been canceled.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
2. Claim 1 recites the limitation "the first source and drain regions" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
2. Claims 1, 2, 3, 4, 5, 6, 12, 13, 14, 15, 16, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Nayak (US 6,372,590).
With respect to claims 1, 2, 3, 4, 12, 13, 14, 15, 16, 17, and 18, AAPA teaches a method for manufacturing a semiconductor device, comprising steps of (see the Background of Invention of this application):
forming source and drain regions in an upper surface of a SiGe-based substrate, the source and drain regions containing an n-type impurity.

AAPA fails to teach forming source and drain extension regions in the upper surface of substrate and implanting nitrogen into the source and drain extension regions.

Nayak teach forming n-type source and drain extension regions in an upper surface of an substrate and then implanting nitrogen with implantation dose of 1×10^{14} to 5×10^{15} atoms/cm² and implantation energy of 1KeV to 100KeV into the source and drain extension regions to reduce series resistance and hot carrier effects. See the abstract of Nayak.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to form source and drain extension regions in the upper surface of substrate and implant nitrogen with implantation dose of 1×10^{14} to 5×10^{15} atoms/cm² and implantation energy of 1KeV to 100KeV into the source and drain extension regions to obtain above advantages.

With respect to claim 6, AAPA further teaches that the SiGe-based substrate comprises a Si cap layer on a SiGe film on a silicon substrate.

3. Claims 7, 8, 9, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Nayak (US 6,372,590).

With respect to claims 7 and 8, Nayak fails to teach that the peak concentrations of the implanted nitrogen and n-type impurity of the source and drain extension regions are at the same depth from the upper surface of the substrate.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the depth for the peak concentrations of the implanted nitrogen and impurity through routine experimentation and optimization to obtain optimal or desired device performance because the relative depths of the nitrogen and impurity are result-

effective variables and there is no evidence indicating that they are critical or produce any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 9, annealing is well-known to one of ordinary skill in the art of making semiconductor devices.

With respect to claim 10, the annealing temperature and duration are result-effective variables and there is no evidence indicating that they are critical or produce any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 11, AAPA implicitly teaches forming a gate electrode on the upper surface of SiGe-based substrate with a gate oxide film therebetween. See the Background of Invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Long Pham

Primary Examiner

Art Unit 2814

LP